JEDEC STANDARDS

For a more complete list of standards, pls see http:www.jedec.org

Packaging: Handling/Using Moisture Sensitive Devices, etc.

J-STD-020

JOINT IPC/JEDEC STANDARD FOR MOISTURE/REFLOW SENSITIVITY CLASSIFICATION FOR NONHERMETIC SOLID STATE SURFACE-MOUNT DEVICES

This document identifies the classification level of nonhermetic solid-state surface mount devices (SMDs) that are sensitive to moisture-induced stress. It is used to determine what classification level should be used for initial reliability qualification. Once identified, the SMDs can be properly packaged, stored and handled to avoid subsequent thermal and mechanical damage during the assembly solder reflow attachment and/or repair operation. This revision now covers components to be processed at higher temperatures for lead-free assembly.

J-STD-033

JOINT IPC/JEDEC STANDARD FOR HANDLING, PACKING, SHIPPING AND USE OF MOISTURE/REFLOW SENSITIVE SURFACE-MOUNT DEVICES

This document provides SMD manufacturers and users with standardized methods for handling, packing, shipping and use of moisture/reflow sensitive SMDs. Now updated to support components that may need to be processed at higher temperatures, such as lead-free processes, these methods help avoid damage from moisture absorption and exposure to solder reflow temperatures that can result in yield and reliability degradation. IPC/JEDEC J-STD-033A helps achieve safe and damage-free reflow with the dry packing process and provides a minimum shelf life of 12 months from the seal date when using sealed dry bags.

J-STD-035

JOINT IPC/JEDEC STANDARD FOR ACOUSTIC MICROSCOPY FOR NONHERMETRIC ENCAPSULATED ELECTRONIC COMPONENTS

This standard defines the procedures for performing acoustic microscopy on non-hermetic encapsulated electronic components. This method provides users with an acoustic microscopy process reflow for detecting defects non-destructively in plastic packages while achieving reproducibility.

J-STD-002

SOLDERABILITY TESTS FOR COMPONENT LEADS, TERMINATIONS, LUGS, TERMINALS AND WIRES

This document defines a standard test method for evaluating the solderability of the leads or interconnect features of components, as well as lugs, terminals, wires, and other forms of terminations. Solderability is defined as the ability of the termination to form a uniform, smooth, unbroken, film of solder on its surface with excellent adhesion properties.

Reliability Testing: THB, Autoclave, Temp Cycle, Thermal Shock>

JESD22-A100 - CYCLED TEMPERATURE HUMIDITY BIAS LIFE TEST

This document pertains to the Cycled Temperature-Humidity-Bias Life Test, which is performed to evaluate the reliability of non-hermetically packaged solid state devices in humid environments. It employs conditions of temperature cycling, humidity, and bias that accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors that pass through it.

JESD22-A101 - STEADY-STATE TEMPERATURE HUMIDITY BIAS LIFE TEST

This standard establishes a defined method for performing a temperature humidity life test with bias applied. The test is used to evaluate the reliability of non-hermetically packaged solid state devices in humid environments. It employs high temperature and humidity conditions to accelerate the penetration of moisture through external protective material or along interfaces between the external protective coating and conductors or other features which pass through it.

JESD22-A102 - ACCELERATED MOISTURE RESISTANCE - UNBIASED AUTOCLAVE

This standard pertains to the Unbiased Autoclave Test, which is performed to evaluate the moisture resistance of non-hermetically packaged solid state devices. It is a highly accelerated test which employs conditions of pressure, humidity and temperature under condensing conditions to accelerate moisture penetration through the external protective material (encapsulant or seal) of the package or along the interface between the external protective material and the metallic conductors passing through it.

JESD22-A104 - TEMPERATURE CYCLING

This standard provides a method for determining solid state devices' capability to withstand exposure to alternating cycles of extremely high and extremely low temperatures. The worst-case load temperature must reach the specific extremes to ensure proper sample stressing regardless of chamber loading. Definitions are provided for Load, Monitoring Sensor, Worst-Case Load Temperature, and Working Zone.

JESD22-A105 - POWER AND TEMPERATURE CYCLING

This document establishes a method for determining the ability of a device to withstand exposure to alternating cycles of extremely high and extremely low temperatures, with operating biases periodically applied and removed. This test method is considered destructive, and is intended primarily for device qualification.

JESD22-A106 - THERMAL SHOCK

This document defines the requirements of Thermal Shock testing, which is conducted to determine the resistance of a part to exposure to sudden and extreme changes in temperature, as well as its resistance to the alternating exposures to extremely high and low temperatures.

Package Testing: Visual, Solderability, Mechanical, Lead Integrity

JESD22-B100 - PHYSICAL DIMENSION TESTS

The standard provides a method for determining whether the external physical dimensions of the device are in accordance with the applicable procurement document.

JESD22-B101 - EXTERNAL VISUAL INSPECTION

This document pertains to external visual inspection, the purpose of which is to verify that the materials, design, construction, markings, and workmanship of the device are in accordance with the applicable procurement document. External visual is a nondestructive test and applicable for all package types. The test is useful for qualification, process monitor, or lot acceptance.

JESD22-B102 - SOLDERABILITY TESTING

This document defines a standard test method for determining the solderability of device package terminations that are intended to be joined to another surface using solder for the attachment. It also provides optional conditions for

aging and soldering for the purpose of allowing simulation of the soldering process to be used in the device applications. It provides procedures for dip and look solderability testing of through hole, axial and surface mount devices and simulated reflow testing for surface mount packages.

JESD22-B103 - VIBRATION, VARIABLE FREQUENCY TESTING

This standard pertains to the Vibration, Variable Frequency Test Method, which is intended to determine the ability of component(s) to withstand moderate to severe vibration as a result of motion produced by transportation or filed operation of electrical equipment. This is a destructive test that is intended for component qualification.

JESD22-B104 - MECHANICAL SHOCK TEST

This document defines a standard test for determining the suitability of component parts for use in electronic equipment that may be subjected to moderately severe shocks as a result of suddenly applied forces or abrupt changes in motion produced by rough handling, transportation, or field operation. This is a destructive test intended for device qualification, and is normally applicable to cavity-type packages.

JESD22-B105 - LEAD INTEGRITY TEST

This standard provides various tests for determining the integrity of lead/package interfaces and the lead itself when the lead(s) are bent due to faulty board assembly followed by rework of the part for reassembly. For hermetic packages it is recommended that this test be followed by hermeticity tests in accordance with Test Method A109 to determine if there are any adverse effects from the stresses applied to the seals as well as to the leads. This test, including each of its test conditions, is considered destructive and is only recommended for qualification testing. This test is applicable to all through-hole devices and surface-mount devices requiring lead forming by the user.

Package Testing: RTSH, Coplanarity, Flip Chip Pull, WB/Solder Ball Shear

JESD22-B106

RESISTANCE TO SOLDERING TEMPERATURE FOR THROUGH-HOLE MOUNTED DEVICES

This document establishes a standard procedure for determining whether through-hole solid state devices can withstand the effects of the high temperature to which they will be subjected during the soldering of their leads.

JESD22-B107

COPLANARITY TEST FOR SURFACE-MOUNT SEMICONDUCTOR DEVICES

This document defines a standard test for measuring the deviation of the terminals (leads or solder balls) of surface-mount semiconductor devices from perfect coplanarity.

JESD22-B109

FLIP CHIP TENSILE PULL TEST

This document pertains to the Flip Chip Tensile Pull Test Method, which is performed to determine the fracture mode and strength of the solder bump interconnection between the flip chip die and the substrate. It should be used to assess the quality and consistency of the chip-substrate joining process. This test method is a destructive test.

JESD22-B116

WIRE BOND SHEAR TEST

This document establishes a standard procedure for determining the strength of an integrated circuit's wire bond by shearing the bond from the surface it is attached to and measuring the force required to accomplish it. This method serves as an alternative to pulling the wire vertically until the wire separates from one of it's two bonded surfaces. It also provides guidelines for determining an appropriate minimum shear force for gold balls on aluminum alloy bonding surfaces.

JESD22-B117

BALL GRID ARRAY (BGA) BALL SHEAR

This document defines a standard BGA Ball Shear Test method. It defines the terms related to ball shear testing; describes the BGA ball shear test apparatus and procedure; and identifies the BGA ball shear failure modes and their criteria.